Title: DATA ADAPTATION PROTOCOL
Inventor: Mark Smith, Shiping Li and James Pasco-Anderson
Filing Date: September 9, 2003
Serial No: Not Yet Assigned
Docket No: S0031/7001 Customer No. 021127

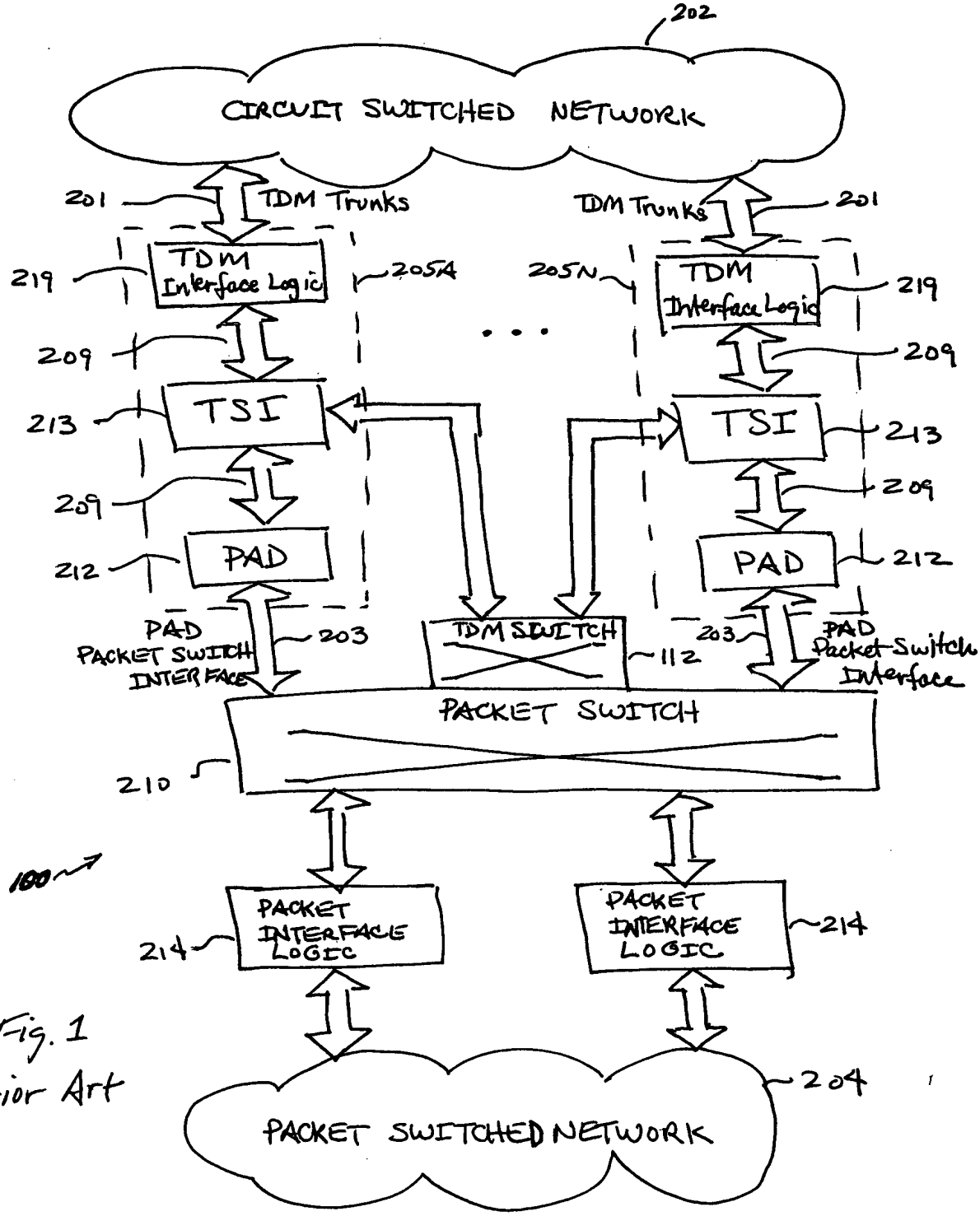


Fig. 1
Prior Art

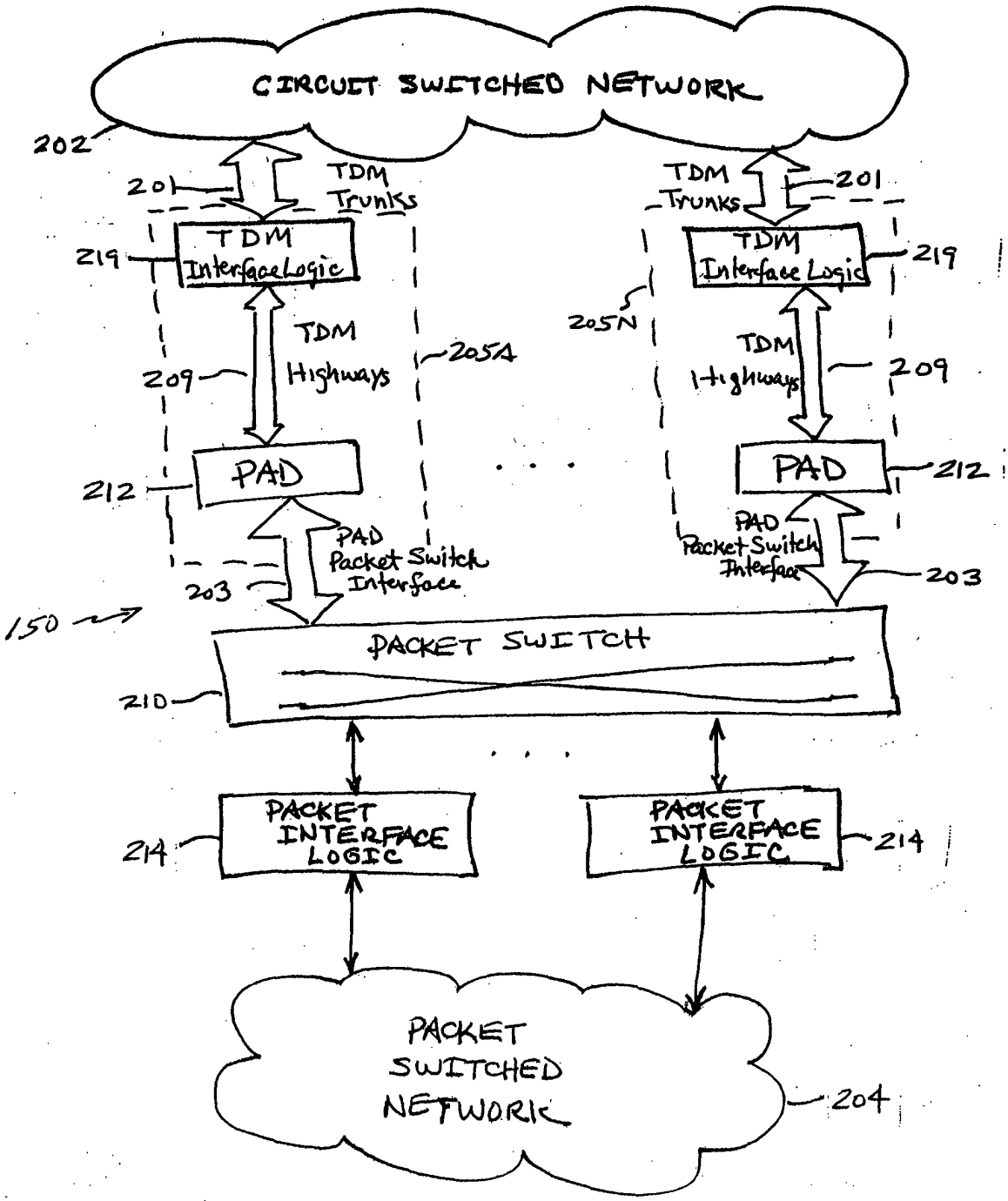


Fig. 2
Prior Art

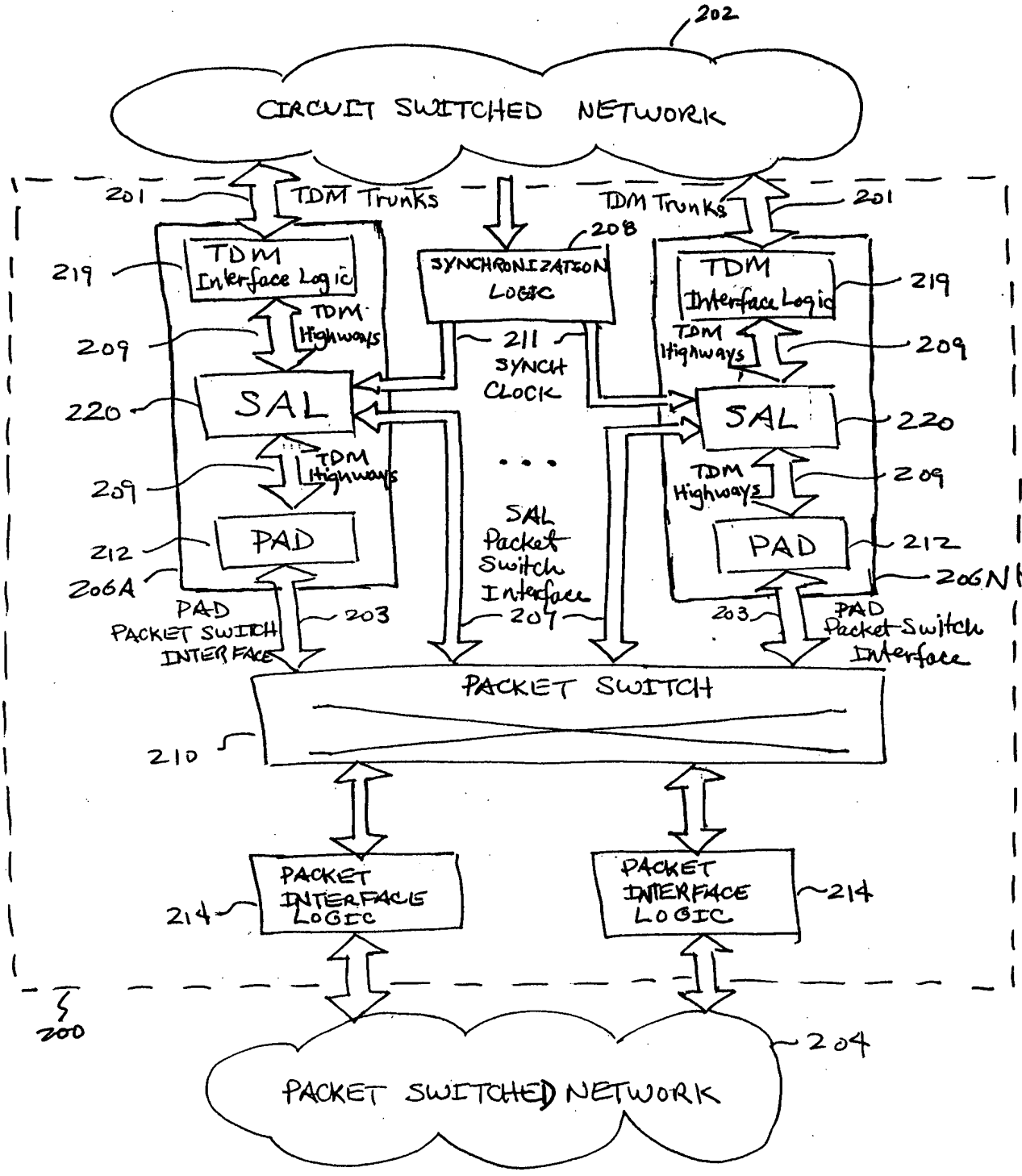

202
CIRCUIT SWITCHED NETWORK
201
TDM Trunks
TDM Trunks
201
208
SYNCHRONIZATION LOGIC
219
TDM Interface Logic
TDM Interface Logic
219
209
TDM Highways
TDM Highways
209
211
SYNCH CLOCK
220
SAL
SAL
220
209
TDM Highways
TDM Highways
209
SAL Packet Switch Interface
207
212
PAD
PAD
212
206A
206N
PAD PACKET SWITCH INTERFACE
203
203
PAD Packet Switch Interface
PACKET SWITCH
210
214
PACKET INTERFACE LOGIC
PACKET INTERFACE LOGIC
214
200
204
PACKET SWITCHED NETWORK

Fig. 3

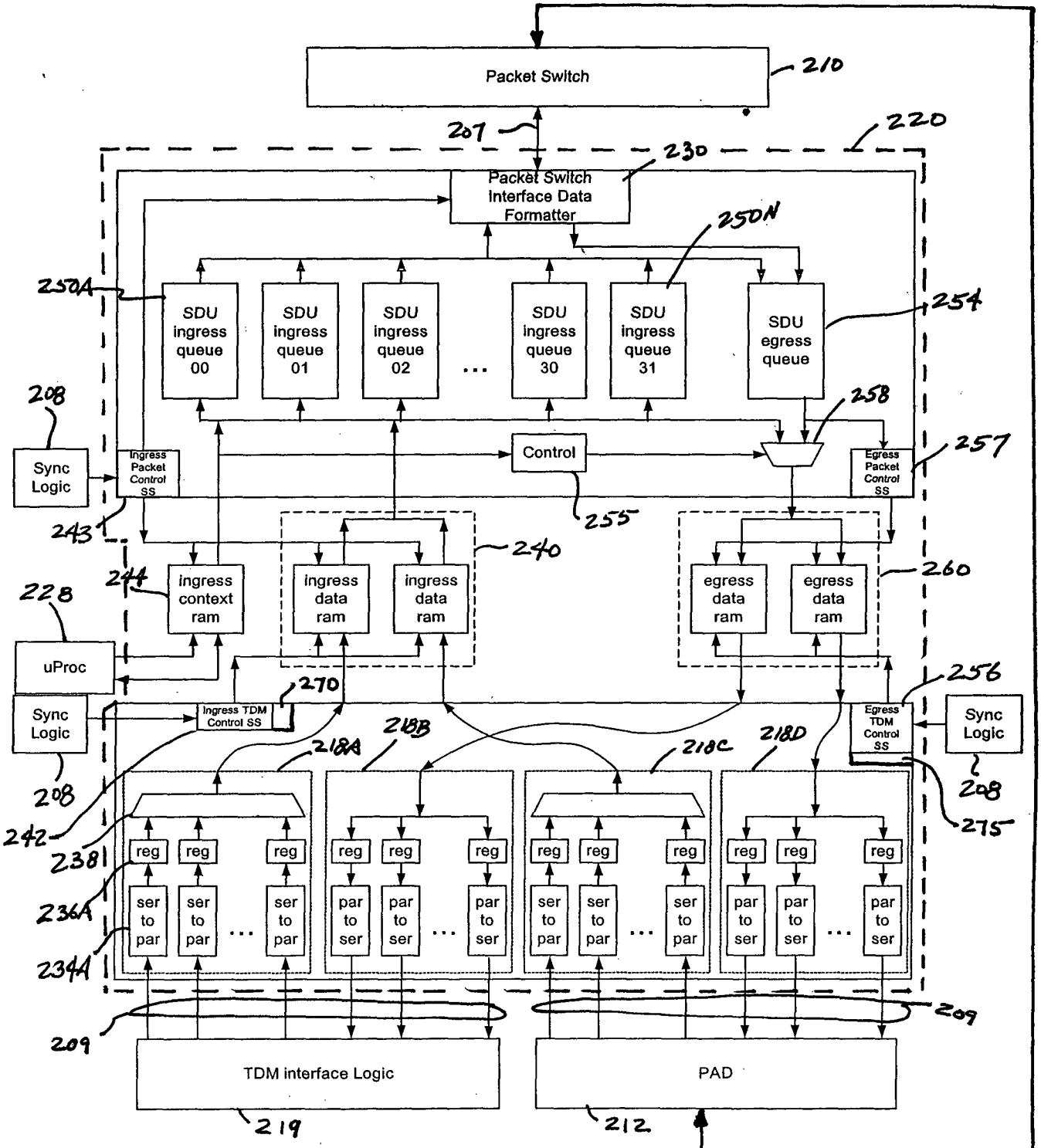

Packet Switch
210
207
220
230
Packet Switch Interface Data Formatter
250N
250A
SDU ingress queue 00
SDU ingress queue 01
SDU ingress queue 02
SDU ingress queue 30
SDU ingress queue 31
SDU egress queue
254
208
Sync Logic
Ingress Packet Control SS
Control
258
257
Egress Packet Control SS
243
255
240
244
ingress context ram
ingress data ram
ingress data ram
egress data ram
egress data ram
260
228
uProc
270
256
Sync Logic
Ingress TDM Control SS
Egress TDM Control SS
Sync Logic
208
208
218A
218B
218C
218D
242
238
236A
234A
275
reg
ser to par
par to ser
209
209
TDM interface Logic
PAD
219
212
203

Fig. 4

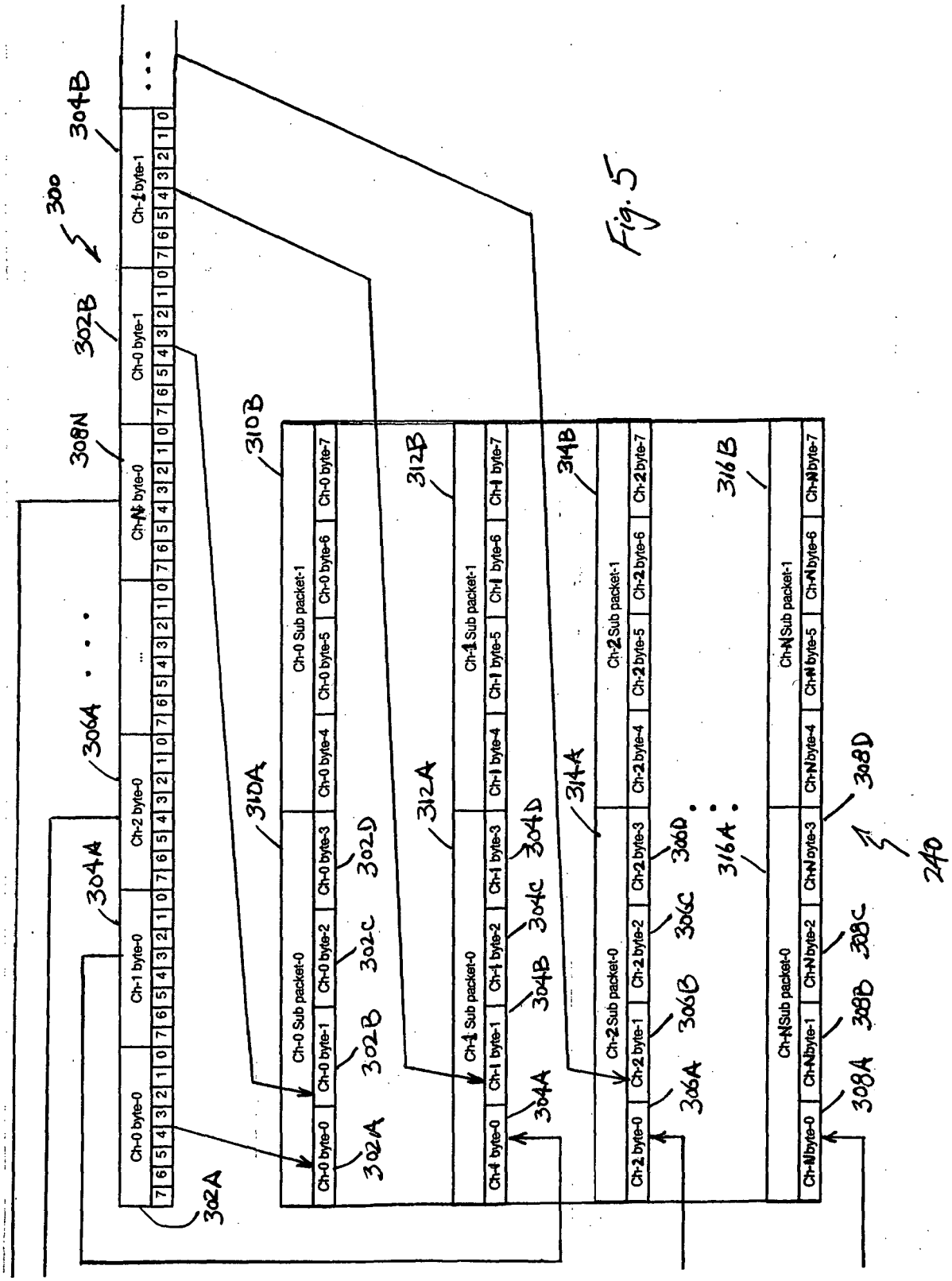

300
302A
302B
302C
302D
304A
304B
304C
304D
306A
306B
306C
306D
308A
308B
308C
308D
308N
310A
310B
312A
312B
314A
314B
316A
316B
240
Ch-0 byte-0
Ch-0 byte-1
Ch-0 byte-2
Ch-0 byte-3
Ch-0 byte-4
Ch-0 byte-5
Ch-0 byte-6
Ch-0 byte-7
Ch-0 Sub packet-0
Ch-0 Sub packet-1
Ch-1 byte-0
Ch-1 byte-1
Ch-1 byte-2
Ch-1 byte-3
Ch-1 byte-4
Ch-1 byte-5
Ch-1 byte-6
Ch-1 byte-7
Ch-1 Sub packet-0
Ch-1 Sub packet-1
Ch-2 byte-0
Ch-2 byte-1
Ch-2 byte-2
Ch-2 byte-3
Ch-2 byte-4
Ch-2 byte-5
Ch-2 byte-6
Ch-2 byte-7
Ch-2 Sub packet-0
Ch-2 Sub packet-1
Ch-N byte-0
Ch-N byte-1
Ch-N byte-2
Ch-N byte-3
Ch-N byte-4
Ch-N byte-5
Ch-N byte-6
Ch-N byte-7
Ch-N Sub packet-0
Ch-N Sub packet-1

Fig. 5

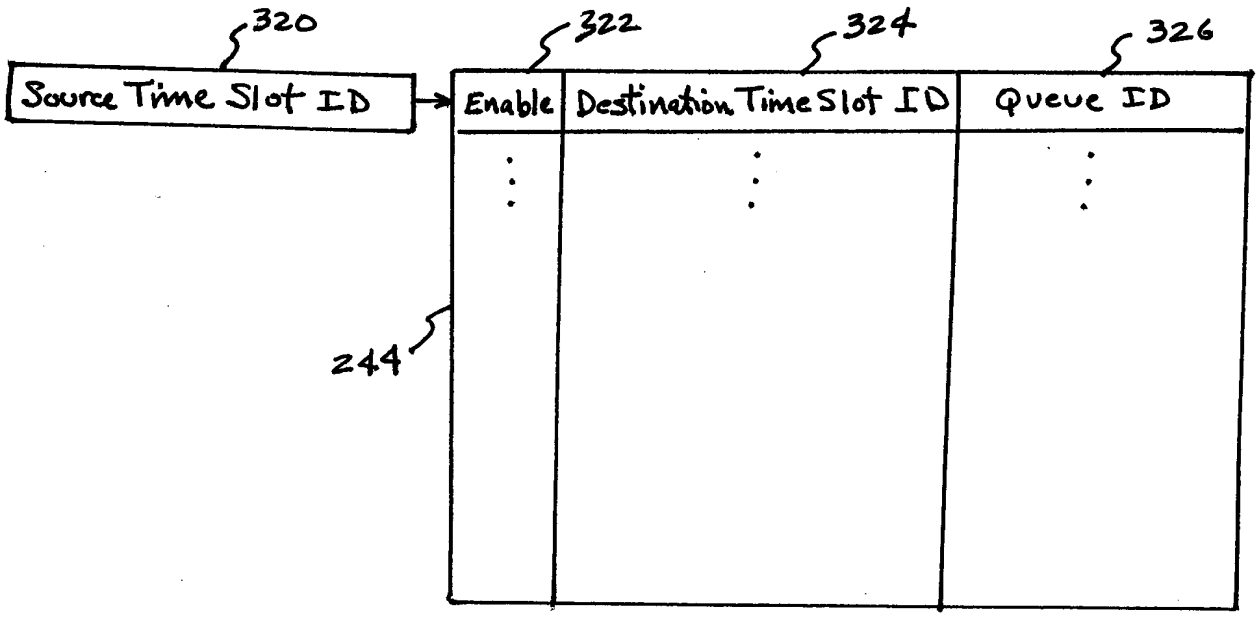

320
322
324
326
Source Time Slot ID
Enable
Destination Time Slot ID
Queue ID
244

Fig. 6

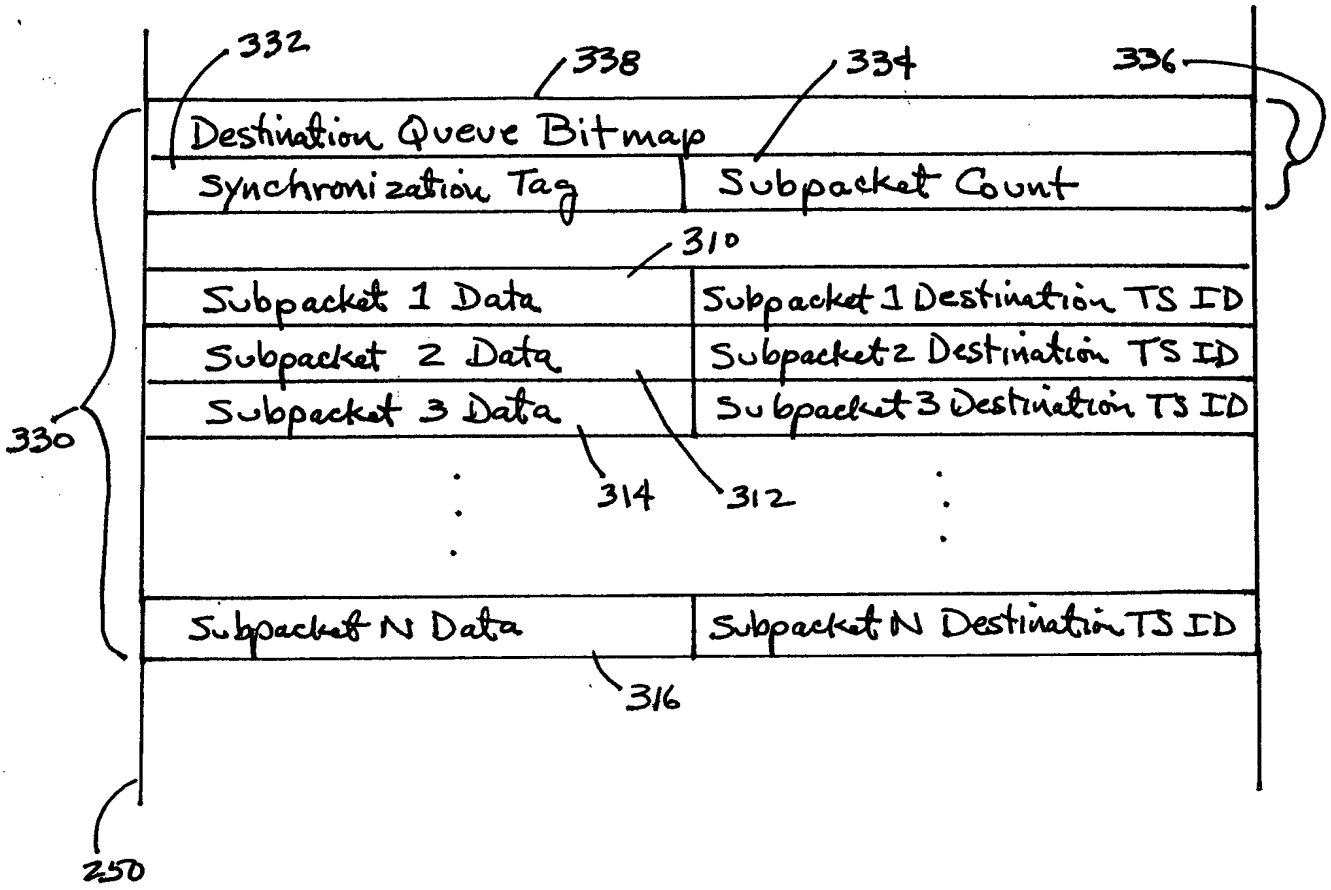

332
338
334
336
Destination Queue Bitmap
Synchronization Tag
Subpacket Count
310
Subpacket 1 Data
Subpacket 1 Destination TS ID
Subpacket 2 Data
Subpacket 2 Destination TS ID
Subpacket 3 Data
Subpacket 3 Destination TS ID
330
314
312
Subpacket N Data
Subpacket N Destination TS ID
316
250

Fig. 7

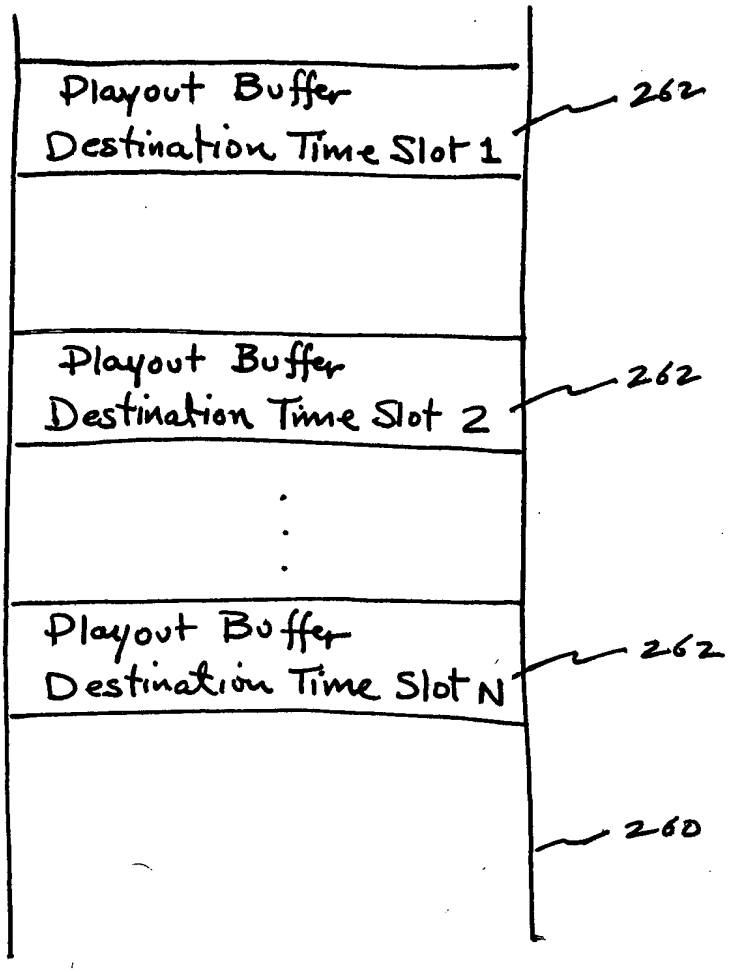

Playout Buffer
Destination Time Slot 1
262
Playout Buffer
Destination Time Slot 2
262
Playout Buffer
Destination Time Slot N
262
260

Fig. 8

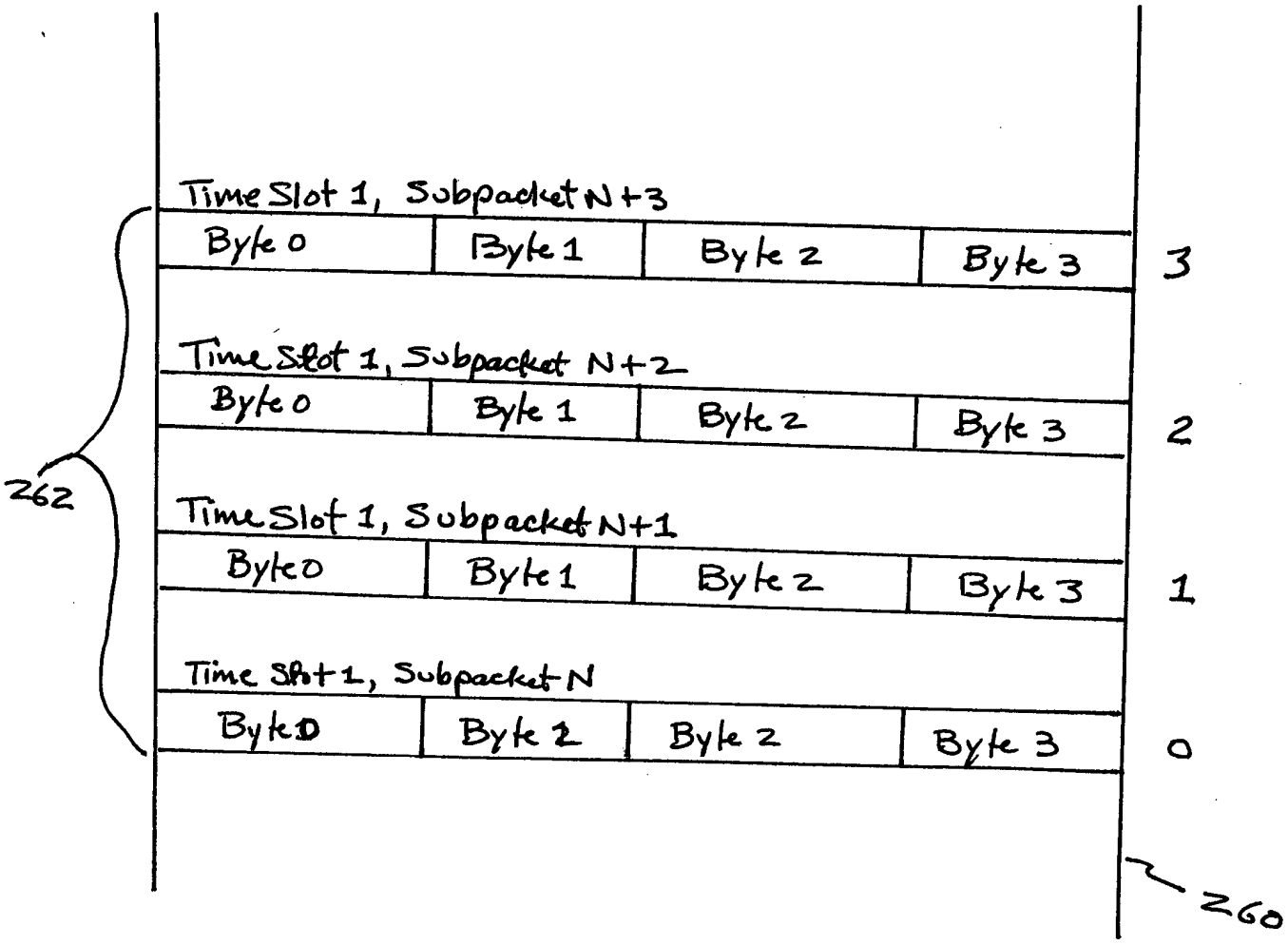
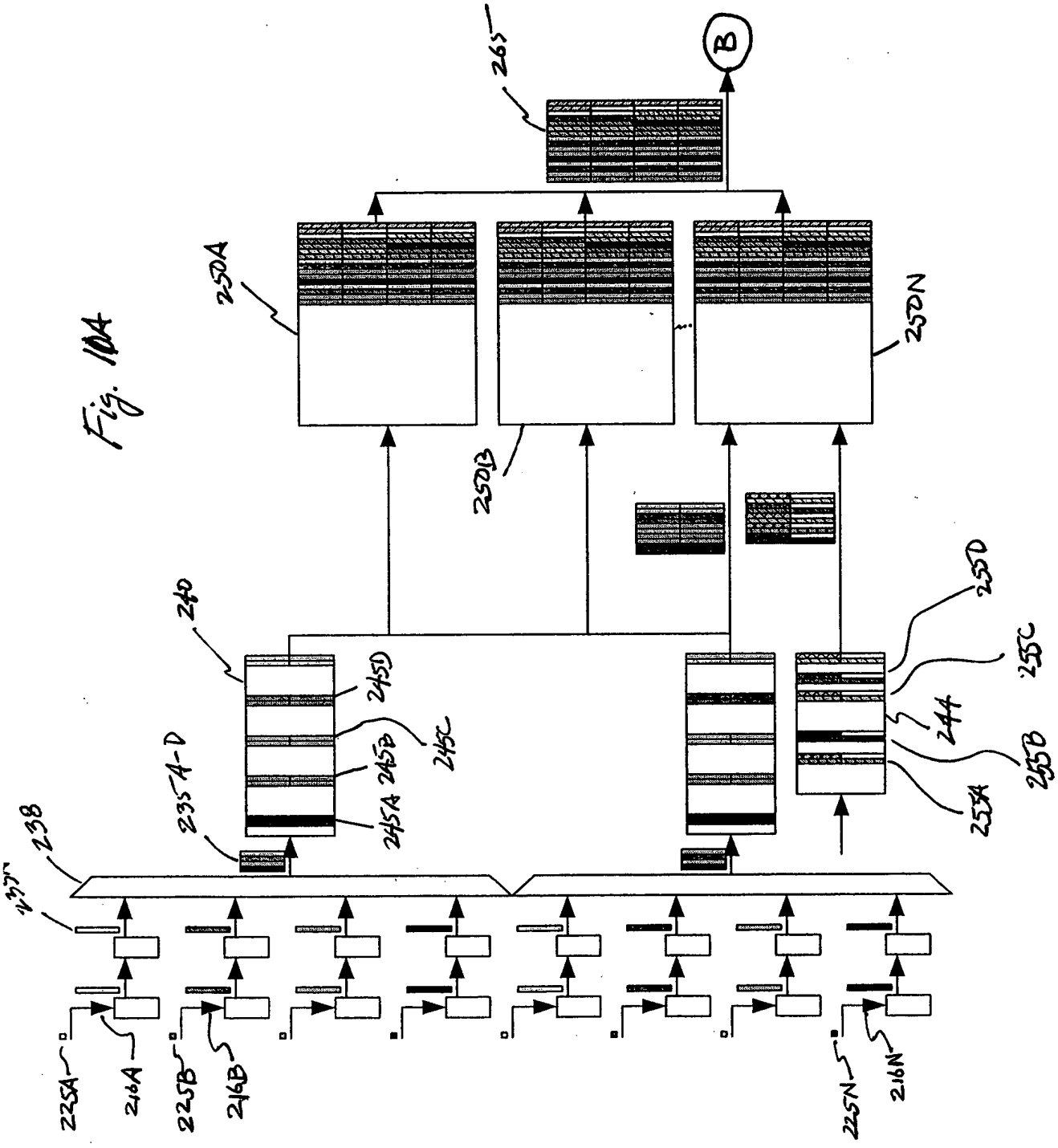

Time Slot 1, Subpacket N+3
Byte 0
Byte 1
Byte 2
Byte 3
3
Time Slot 1, Subpacket N+2
Byte 0
Byte 1
Byte 2
Byte 3
2
Time Slot 1, Subpacket N+1
Byte 0
Byte 1
Byte 2
Byte 3
1
Time Slot 1, Subpacket N
Byte 0
Byte 1
Byte 2
Byte 3
0
262
260

Fig. 9

Fig. 10A


B
265
250A
250B
250N
240
245D
245C
245B
245A
235A-D
238
255D
255C
244
255B
255A
225A
216A
225B
216B
225N
216N

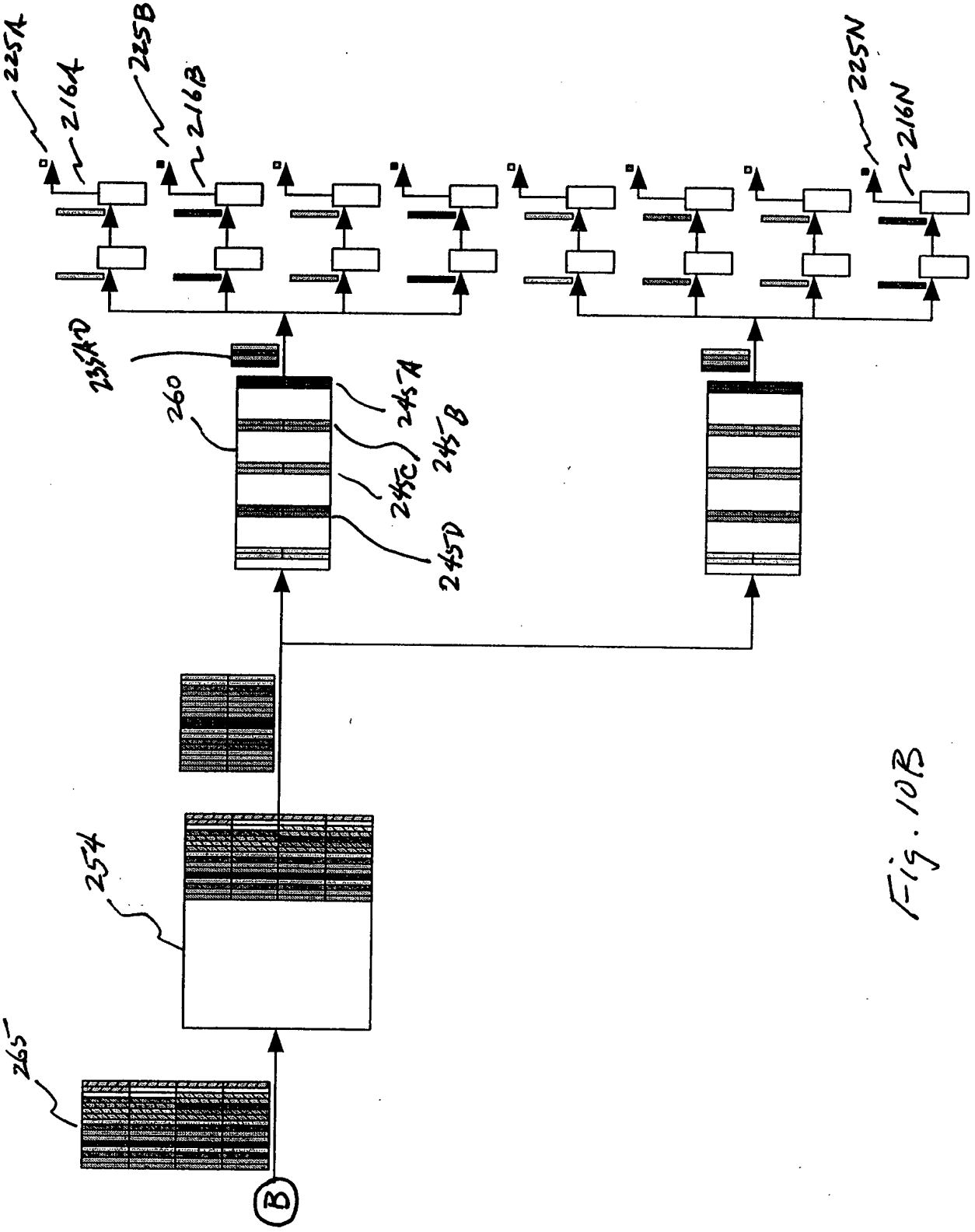

225A
216A
225B
216B
225N
216N
235AD
260
245A
245B
245C
245D
254
265
B

Fig. 10B

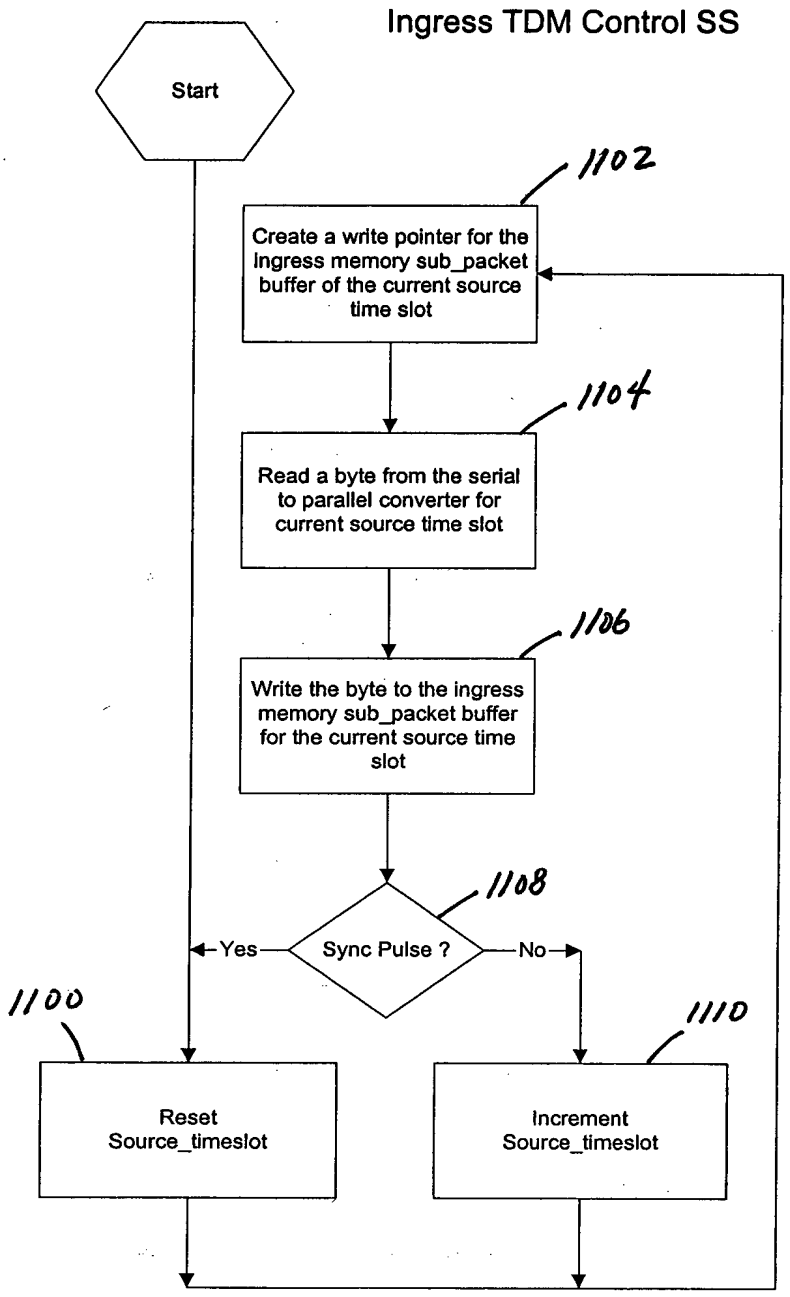

Ingress TDM Control SS
Start
1102
Create a write pointer for the Ingress memory sub_packet buffer of the current source time slot
1104
Read a byte from the serial to parallel converter for current source time slot
1106
Write the byte to the ingress memory sub_packet buffer for the current source time slot
1108
Sync Pulse ?
Yes
No
1100
Reset Source_timeslot
1110
Increment Source_timeslot

Fig. 11

13/15

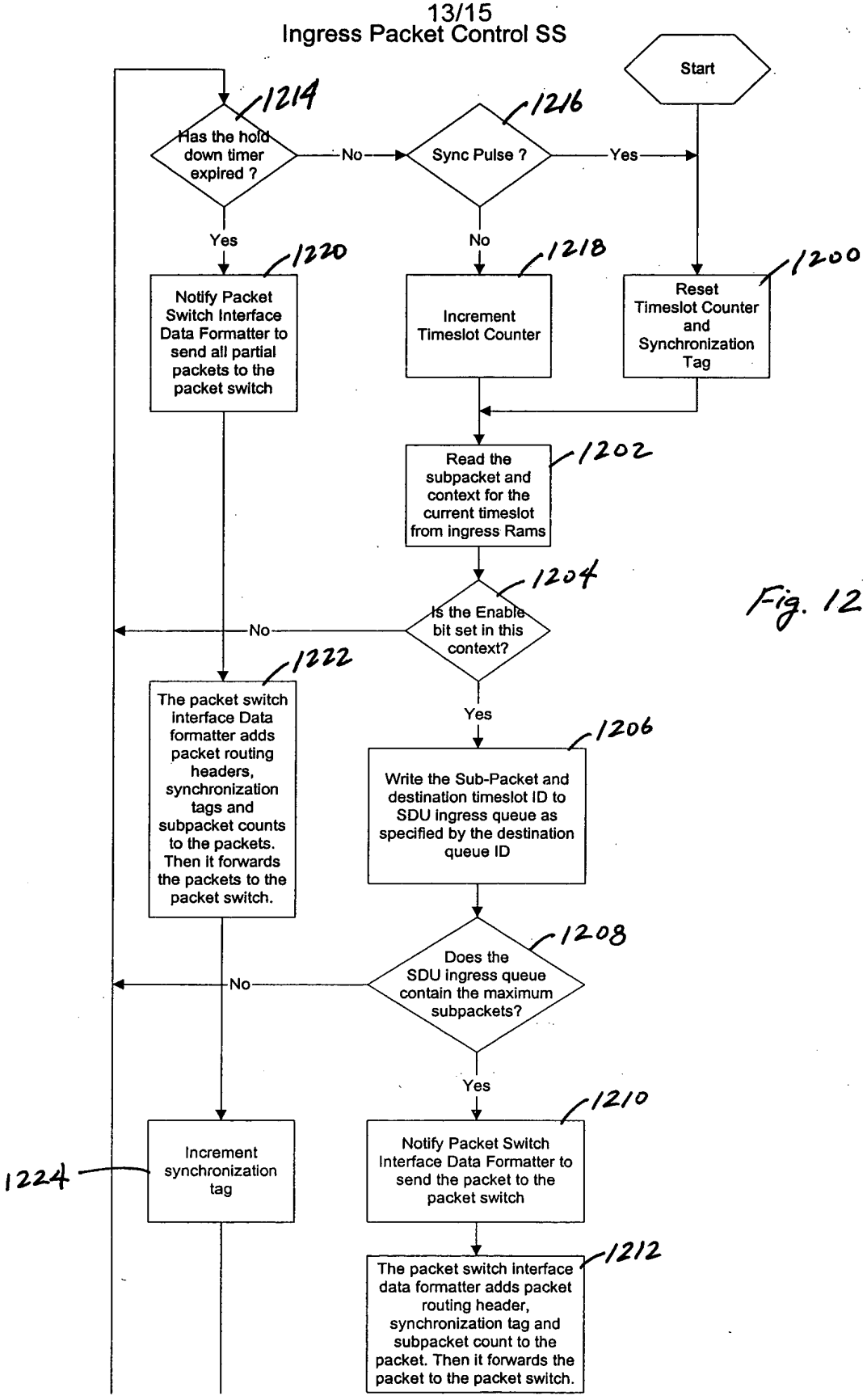

Ingress Packet Control SS
Start
1214
Has the hold down timer expired ?
No
1216
Sync Pulse ?
Yes
Yes
No
1220
Notify Packet Switch Interface Data Formatter to send all partial packets to the packet switch
1218
Increment Timeslot Counter
1200
Reset Timeslot Counter and Synchronization Tag
1202
Read the subpacket and context for the current timeslot from ingress Rams
1204
Is the Enable bit set in this context?
No
Yes
1222
The packet switch interface Data formatter adds packet routing headers, synchronization tags and subpacket counts to the packets. Then it forwards the packets to the packet switch.
1206
Write the Sub-Packet and destination timeslot ID to SDU ingress queue as specified by the destination queue ID
1208
Does the SDU ingress queue contain the maximum subpackets?
No
Yes
1224
Increment synchronization tag
1210
Notify Packet Switch Interface Data Formatter to send the packet to the packet switch
1212
The packet switch interface data formatter adds packet routing header, synchronization tag and subpacket count to the packet. Then it forwards the packet to the packet switch.

Fig. 12

Egress Packet Control SS

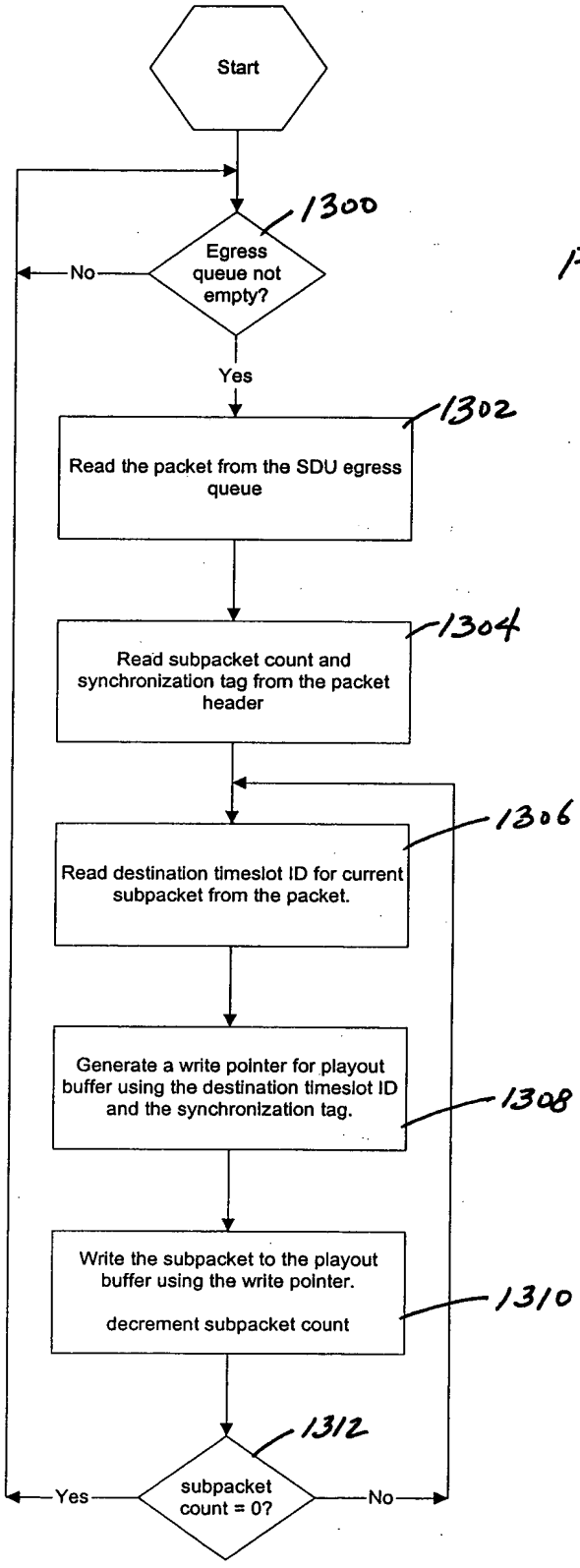


Fig. 13

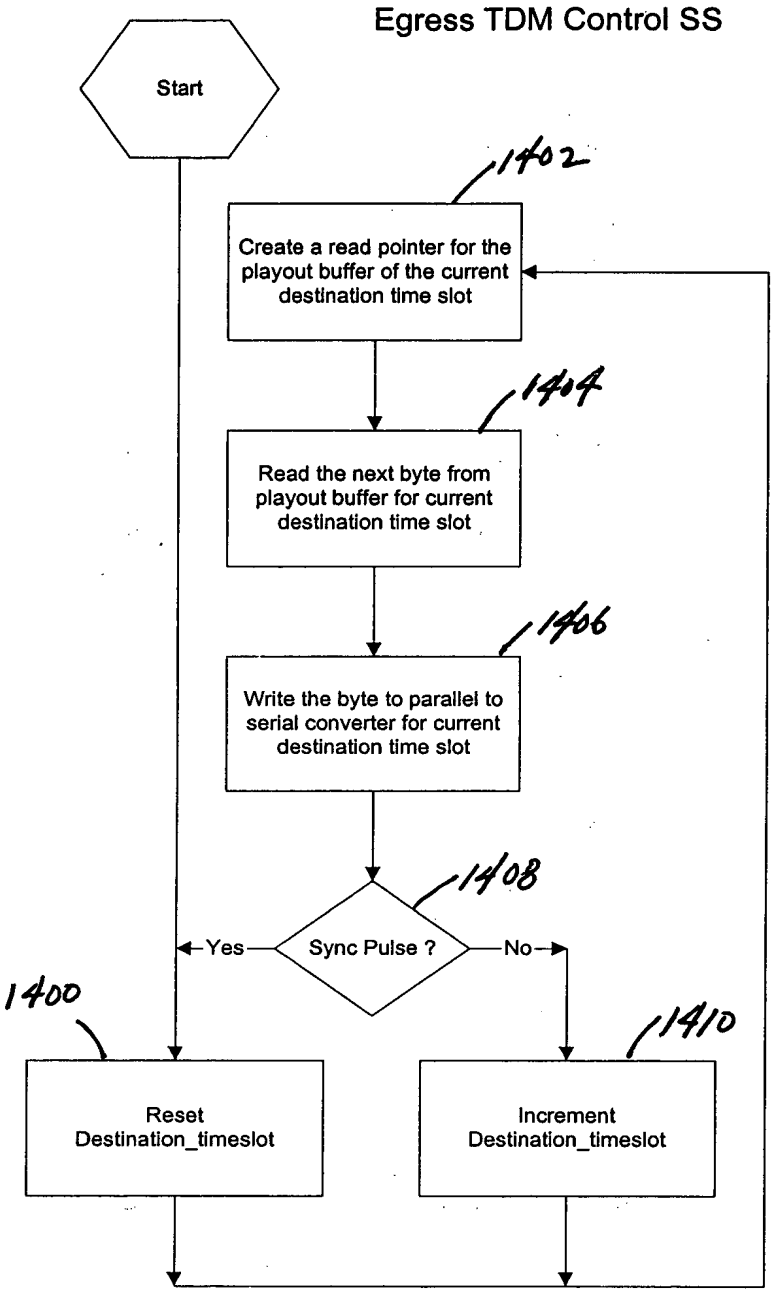

Egress TDM Control SS
Start
1402
Create a read pointer for the playout buffer of the current destination time slot
1404
Read the next byte from playout buffer for current destination time slot
1406
Write the byte to parallel to serial converter for current destination time slot
1408
Sync Pulse ?
Yes
No
1400
Reset Destination_timeslot
1410
Increment Destination_timeslot

Fig. 14